REMARKS

This responds to the Office Action mailed on October 7, 2008.

No claims are amended, no claims are canceled, and no claims are added; thus, claims 1-15, 17-20 and 28-33 are now pending in this application.

§103 Rejection of the Claims

Claims 1-9 and 28-33 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Shiraki (U.S. 6,969,808) in view of Johnson et al. (U.S. 6,469,530), hereinafter "Johnson". Applicant respectfully traverses.

Applicant submits the rejection fails to make a *prima facie* case of obviousness because the asserted combination of Shiraki and Johnson fails to teach all elements of the claimed subject matter.

Claims 1-9

Independent claim 1 recites, among other things, "a plated through hole attached to the plane metallization layer and terminating at the at least one of the first major exterior surface and the second major exterior surface including the plurality of component mounting pads" and "a circuit tester for determining if a current will flow between the pad and the signal carrying via, and the plane metallization layer to test the spacing of a plane metallization layer from a signal through hole that passes through the plane metallization layer".

Applicant respectfully submits that the Examiner has made an improper *prima facie* showing of obviousness at least because the Examiner's proposed combination of Shiraki and Johnson fails to teach or suggest an arrangement "to test the spacing of a plane metallization layer from a signal through hole that passes through the plane metallization layer", as recited in claim 1.

The Examiner admits that Shiraki does not teach a circuit tester for determining if a current will flow between the pad and the signal carrying via, and the plane metallization layer to test the spacing of a plane metallization layer from a signal through hole that passes through the plane metallization layer. (See page 3 of the Office Action dated October 7, 2008). The Examiner asserts that Johnson teaches the missing element. Applicant respectfully disagrees.

Johnson relates to a BGA Probe Array (col. 6, lines 41-49) to connect to a BGA package containing one or more integrated circuits. The BGA probe array(30) connects to a BGA package mounted to a PCB to provide input/output connections for in-circuit testing and debugging of the circuits in the BGA package (Johnson; col. 4, lines 39-46; col.6, lines 41-49), thus, Applicant submits the Probe Array of Johnson is merely a connector for connecting equipment used in testing the BGA package. Applicant is unable to find in Johnson a teaching or fair suggestion that the probe array of Johnson can be combined with a device, such as the device of Shiraki, to test the spacing of a plane metallization layer from a signal through hole that passes through the plane metallization layer of the device, as recited in claim 1.

Based on the above, Applicant is unable to find in the asserted combination of Shiraki and Johnson fails to teach the above quoted feaures of claim 1, such as, a device comprising, among other things, a circuit tester for testing the spacing between the plane metallization layer and the pad associated with the signal carrying through hole as recited in claim 1.

In addition, Applicant is unable to find any motivation for combining Shiraki and Johnson as proposed by the Examiner to achieve Applicant's inventive subject matter because neither Shiraki nor Johnson teaches an arrangement to test the spacing of a plane metallization layer from a signal through hole that passes through the plane metallization layer, as recited in claim 1. Notwithstanding the forgoing, the Examiner appears to use hindsight to propose the combination of Shiraki and Johnson based on Applicant's disclosure.

Even if one were to find proper motivation to combine Shiraki and Johnson, there would be no reasonable expectation of success, as required to make a proper prima facie case of obviousness. Shiraki teaches a grid of equally spaced through-holes 41 that attach to either a power plane metallization layer or a ground plane metallization layer. Shiraki also teaches land 31 connected to the end of the through hole for the signal carrying line. However, land 31 is not spaced on the same grid. Rather, land 31 is spaced between four of the equally spaced through-holes. Thus, in Shiraki, land 31 is not on the grid of equally spaced through-holes. In contrast, Johnson teaches a uniform grid separation of the probes. [See Johnson FIGS. 2A and 2B and col. 9, lines 53-61]. Therefore, even if one were to combine Shiraki and Johnson as proposed by the Examiner, the equally spaced grid of Johnson would not electrically contact land 31 of

Shiraki because land 31 is not positioned on a grid. Thus, the proposed combination of Shiraki and Johnson would not work.

Therefore, Applicant respectfully requests withdrawal of the rejection and reconsideration and allowance of claim 1.

Claims 2-8 depend either directly or indirectly on independent claim 1 and are believed to be in condition for allowance at least for the reasons provided with respect to independent claim 1.

Claims 28-33

Independent claim 28 recites, among other things, features analogous to claim 1, such as "a test device electrically coupled to the feature for testing the spacing between the feature and the plane metallization layer". Thus, for at least the reasons presented above regarding claim 1, Applicant is unable to find in Johnson a teaching or fair suggestion that the probe array of Johnson can be combined with a device, such as the device of Shiraki, for testing the spacing between the feature and the plane metallization layer, as recited in claim 28.

Accordingly, Applicant requests reversal of the rejection and allowance of claim 28. Claims 29-33 depend from claim 28 and include the things of claim 28. Thus, Applicant submits that claims 29-33 are also in patentable condition for at least the reasons present above regarding claim 28. Accordingly, Applicant requests reversal of the rejection and allowance of claims 29-33.

Claims 10-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Shiraki (U.S. 6,969,808) in view of Conn et al. (U.S. 5,418,690), and further in view of Johnson et al. (U.S. 6,469,530). Applicant respectfully traverses the rejection.

Independent claim 10 recites, among other things, features analogous to claim 1, such as, "a plated through hole attached to the plane metallization layer and terminating at the at least one of the first major exterior surface and the second major exterior surface including the plurality of component mounting pads, the plated through hole attached to the plane metallization layer electrically isolated from the plurality of component mounting pads" and "a circuit test apparatus for testing the spacing between the plane metallization layer and the pad associated with the

signal carrying through hole". Thus, for at least the reasons presented above regarding claim 1, Applicant is unable to find in Johnson a teaching or fair suggestion that the probe array of Johnson can be combined with a device, such as the device of Shiraki or Conn et al., or both, to include a circuit test apparatus for testing the spacing between the plane metallization layer and the pad associated with the signal carrying through hole, as recited in claim 10. Thus, Applicant respectfully submits that the proposed combination of Shiraki, Conn et al., and Johnson fails to teach or suggest "a circuit test apparatus for testing the spacing between the plane metallization layer and the pad associated with the signal carrying through hole", as recited in claim 10.

Applicant respectfully requests withdrawal of the rejection and reconsideration and allowance of claim 10.

Claims 11-15 depend either directly or indirectly on independent claim 10 and are believed to be in condition for allowance at least for the reasons provided with respect to independent claim 10.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's representative at (612) 373-6969 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on February 9, 2009.

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